# METHOD AND APPARATUS FOR VISUALIZATION OF MICROPROCESSOR PIPELINE OPERATION

## Abstract

A method and apparatus of visualizing events within a microprocessor include simulating the operation of a microprocessor for a set of instructions, generating the internal state information from the simulation and graphically displaying an execution behavior based on the internal state information. The graphical display represents a flow of the instructions through an internal pipeline in the microprocessor. Execution behavior is selectively displayed based on type of behavior and clock cycle the execution occurred during on the microprocessor. A log of the execution behavior of the set of instructions on the microprocessor is created. The set of instructions is created from a graphical display of selectable instructions.

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